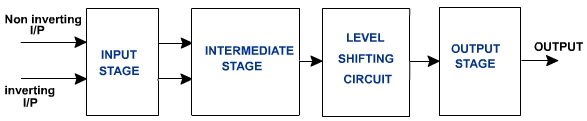
**The operational amplifier**

An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential (OPAMP) amplifiers and followed by a level translator and an output stage. An operational amplifier is available as a single integrated circuit package.

The block diagram of OPAMP is shown in **fig. 1**.

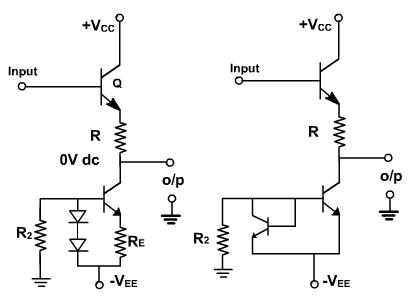
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**Fig. 1**

The input stage is a dual input balanced output differential amplifier. This stage provides most of the voltage gain of the amplifier and also establishes the input resistance of the OPAMP.The intermediate stage of OPAMP is another differential amplifier which is driven by the output of the first stage. This is usually dual input unbalanced output.

Because direct coupling is used, the dc voltage level at the output of intermediate stage is well above ground potential. Therefore level shifting circuit is used to shift the dc level at the output downward to zero with respect to ground. The output stage is generally a push pull complementary amplifier. The output stage increases the output voltage swing and raises the current supplying capability of the OPAMP. It also provides low output resistance.

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| **Level Translator:**  Because of the direct coupling the dc level at the emitter rises from stages to stage. This increase in dc level tends to shift the operating point of the succeeding stages and therefore limits the output voltage swing and may even distort the output signal.  To shift the output dc level to zero, level translator circuits are used. An emitter follower with voltage divider is the simplest form of level translator as shown in **fig. 2**.  Thus a dc voltage at the base of Q produces 0V dc at the output. It is decided by R1 and R2. Instead of voltage divider emitter follower either with diode current bias or current mirror bias as shown in **fig. 3**may be used to get better results.  In this case, level shifter, which is common collector amplifier, shifts the level by 0.7V. If this shift is not sufficient, the output may be taken at the junction of two resistors in the emitter leg. | https://nptel.ac.in/content/storage2/courses/117107094/lecturers/lecture_5/images/fig12.jpg  **Fig. 2** |



**Fig. 3**

|  |
| --- |
| **Practical Operational Amplifier** |
| The symbolic diagram of an OPAMP is shown in **fig. 1**.  **https://nptel.ac.in/content/storage2/courses/117107094/lecturers/lecture_6/images/fig1.jpg**  741c is most commonly used OPAMP available in IC package. It is an 8-pin DIP chip.  **Parameters of OPAMP:**  The various important parameters of OPAMP are follows:  **1.Input Offset Voltage:**   |  |  | | --- | --- | | Input offset voltage is defined as the voltage that must be applied between the two input terminals of an OPAMP to null or zero the output **fig. 2**, shows that two dc voltages are applied to input terminals to make the output zero.  Vio = Vdc1 – Vdc2  Vdc1 and Vdc2 are dc voltages and RS represents the source resistance. Vio is the difference of Vdc1 and Vdc2. It may be positive or negative. For a 741C OPAMP the maximum value of Vio is 6mV. It means a voltage ± 6 mV is required to one of the input to reduce the output offset voltage to zero. The smaller the input offset voltage the better the differential amplifier, because its transistors are more closely matched. | https://nptel.ac.in/content/storage2/courses/117107094/lecturers/lecture_6/images/fig15.jpg  **Fig. 2** |   **2. Input offset Current:**  The input offset current Iio is the difference between the currents into inverting and non-inverting terminals of a balanced amplifier.  Iio = |   IB1 – IB2 |  The Iio for the 741C is 200nA maximum. As the matching between two input terminals is improved, the difference between IB1 and IB2 becomes smaller, i.e. the Iio value decreases further.For a precision OPAMP 741C, Iio is 6 nA  **3.Input Bias Current:**  The input bias current IB is the average of the current entering the input terminals of a balanced amplifier i.e.  IB = (IB1 + IB2 ) / 2  For 741C IB(max) = 700 nA and for precision 741C IB = ± 7 nA  **4. Differential Input Resistance: (Ri)**  Ri is the equivalent resistance that can be measured at either the inverting or non-inverting input terminal with the other terminal grounded. For the 741C the input resistance is relatively high 2 MΩ. For some OPAMP it may be up to 1000 G ohm.  **5. Input Capacitance: (Ci)**  Ci is the equivalent capacitance that can be measured at either the inverting and noninverting terminal with the other terminal connected to ground. A typical value of Ci is 1.4 pf for the 741C.  **6. Offset Voltage Adjustment Range:**  741 OPAMP have offset voltage null capability. Pins 1 and 5 are marked offset null for this purpose. It can be done by connecting 10 K ohm pot between 1 and 5 as shown in**fig. 3**.  https://nptel.ac.in/content/storage2/courses/117107094/lecturers/lecture_6/images/fig16.jpg  **Fig. 3**  By varying the potentiometer, output offset voltage (with inputs grounded) can be reduced to zero volts. Thus the offset voltage adjustment range is the range through which the input offset voltage can be adjusted by varying 10 K pot. For the 741C the offset voltage adjustment range is ± 15 mV. |

**Parameters of OPAMP:**

**7. Input Voltage Range :**

Input voltage range is the range of a common mode input signal for which a differential amplifier remains linear. It is used to determine the degree of matching between the inverting and noninverting input terminals. For the 741C, the range of the input common mode voltage is ± 13V maximum. This means that the common mode voltage applied at both input terminals can be as high as +13V or as low as –13V.

**8. Common Mode Rejection Ratio­ (CMRR).**

CMRR is defined as the ratio of the differential voltage gain Ad to the common mode voltage gain ACM

CMRR = Ad / ACM.

For the 741C, CMRR is 90 dB typically. The higher the value of CMRR the better is the matching between two input terminals and the smaller is the output common mode voltage.

**9. Supply voltage Rejection Ratio: (SVRR)**

SVRR is the ratio of the change in the input offset voltage to the corresponding change in power supply voltages. This is expressed in V / V or in decibels, SVRR can be defined as

SVRR = Vio /  V

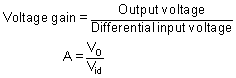
Where  V is the change in the input supply voltage and Vio is the corresponding change in the offset voltage.

For the 741C, SVRR = 150 µ V / V.

For 741C, SVRR is measured for both supply magnitudes increasing or decreasing simultaneously, with R3 10K. For same OPAMPS, SVRR is separately specified as positive SVRR and negative SVRR.

**10. Large Signal Voltage Gain:**

Since the OPAMP amplifies difference voltage between two input terminals, the voltage gain of the amplifier is defined as



Because output signal amplitude is much large than the input signal the voltage gain is commonly called large signal voltage gain. For 741C is voltage gain is 200,000 typically.

**11. Output voltage Swing:**

The ac output compliance PP is the maximum unclipped peak to peak output voltage that an OPAMP can produce. Since the quiescent output is ideally zero, the ac output voltage can swing positive or negative. This also indicates the values of positive and negative saturation voltages of the OPAMP. The output voltage never exceeds these limits for a given supply voltages +VCC and –VEE. For a 741C it is ± 13 V.

**12. Output Resistance: (RO)**

RO is the equivalent resistance that can be measured between the output terminal of the OPAMP and the ground. It is 75 ohm for the 741C OPAMP.

13. **Slew Rate:**

Slew rate is defined as the maximum rate of change of output voltage per unit of time under large signal conditions and is expressed in volts /  secs.

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